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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,621	08/19/2003	Ric Howard	065324-0028	7506

34756 7590 03/24/2006

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EXAMINER	
MCLEAN MAYO, KIMBERLY N	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 03/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,621	HOWARD ET AL.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *49* is/are allowed.

6)☒ Claim(s) *1-8, 12-19, 23-28, 32-40 and 44-48* is/are rejected.

7)☒ Claim(s) *9-11,20-22,29-31 and 41-43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The enclosed detailed action is in response to the Application submitted on August 19, 2003.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-2, 4, 12-13 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Carlson et al. (USPN: 6,807,590).

Regarding claims 1 and 4, Carlson discloses while providing independent and asynchronous performance of a memory read process of a plurality of processes, providing independent and asynchronous performance of a write process of a plurality of processes, wherein the write process comprises obtaining [reading/polling] a first copy of a memory full indicator (C 8, L 54-55); obtaining [reading] a copy of a read index [address], the read index copy indicating a read element position in the memory (C 8, L 15-16; free space counter reads the read index); when the first copy of the memory full indicator indicates that the memory is not full (Figure 4, step 406), determining an available write count from the read index copy and a write index, the write index

indicating a write element position in the memory (C 8, L 15-20; Figure 4, step 408); beginning at the write element position, writing an amount of data corresponding to the available write count (C 8, L 11-13; Figure 4, step 420); updating the write index to indicate a next write element position based upon the amount of data written (inherent; in FIFO operations, updating of the write index is required to ensure that the next data written does not overwrite the data written previously and the properly determine memory fullness).

Regarding claim 2, Carlson discloses determining whether the updated write index is equal to the read index (Figure 4, step 406; the steps indicated in Figure 4 occur on each write request, thus for a subsequent write request, the system will perform step 406 again).

Regarding claims 12 and 15, Carlson discloses a memory (Figure 3, Reference 306; the memory is internal to Reference 106 in Figures 1 and 2); a first node coupled to the memory, the first node capable of independently and asynchronously performing a read process of the plurality of processes (Figure 1, Reference 100); and a second node coupled to the memory (Figure 1, Reference 106 and the other devices coupled to Reference 108), the second node capable of independently and asynchronously performing a memory write process, of the plurality of processes, by obtaining [reading/polling] a first copy of a memory full indicator (C 8, L 54-55); obtaining [reading] a copy of a read index [address], the read index copy indicating a read element position in the memory (C 8, L 15-16; free space counter reads the read index); when the first copy of the memory full indicator indicates that the memory is not full (Figure 4, step 406), determining an available write count from the read index copy and a write index, the write index

indicating a write element position in the memory (C 8, L 15-20; Figure 4, step 408); beginning at the write element position, writing an amount of data corresponding to the available write count (C 8, L 11-13; Figure 4, step 420); updating the write index to indicate a next write element position based upon the amount of data written (inherent; in FIFO operations, updating of the write index is required to ensure that the next data written does not overwrite the data written previously and the properly determine memory fullness).

Claim 13 is rejected for the same rationale applied to claim 2 above.

4. Claims 1-8, 12-19, 23-28, 32-40 and 44-48 are rejected under 35 U.S.C. 102(b) as being anticipated by L'Ecuyer (USPN: 6,134,629).

Regarding claims 1 and 4, L'Ecuyer discloses while providing independent and asynchronous performance of a memory read process of a plurality of processes, providing independent and asynchronous performance of a write process of a plurality of processes, wherein the write process comprises obtaining a first copy of a memory full indicator (C 7, L 9-17); obtaining a copy of a read index [address], the read index copy indicating a read element position in the memory and when the first copy of the memory full indicator indicates that the memory is not full (C 7, L 16-17), determining an available write count from the read index copy and a write index, the write index indicating a write element position in the memory (C 7, L 16-38; C 4, L 9-67; C 5, L 1-7); beginning at the write element position, writing an amount of data corresponding to the available write count and updating the write index to indicate a next write element position based upon the amount of data written (C 6, L 35-67; C 7, L 1-5).

Regarding claims 2-3, L'Ecuyer write index is equal to the read index and setting the memory full indicator to indicate that the memory is full or may be full (C 7, L 9-12).

Regarding claims 5 and 8, L'Ecuyer discloses obtaining a second copy of the memory full indicator (Figure 3, step 51; the system sets the full flag false, however, in doing so the system establishes that the memory is not full); obtaining a copy of the write index and determining an available read count from the read index and the write index copy (C 5, L 51-67; C 6, L 1-8; C 3, entire); beginning at the read element position, reading an amount of data corresponding to the available read count and updating the read index to indicate a next read element position based on the amount of data read (C 5, L 9-44).

Regarding claims 6-7, L'Ecuyer subsequent to updating the read index, when the second copy of the memory full indicator indicates that the memory is full or may be full, clearing the memory full indicator to indicate that the memory is not full (C 5, L 45-48). Additionally, regarding claim 7, the full flag is cleared after being set, while the write and read index are not equal when step 53 in Figure 3 indicates that the write index and the read index are not equal.

Regarding claims 12 and 23, L'Ecuyer discloses a memory (Figure 1); a first node (process or device coupled to one of the ports of the FIFO memory, which is a finite state machine of some sort since the device is capable of accessing the memory; L'Ecuyer discloses a dual port FIFO; C 1, L 16-18); a second node coupled to the memory (the second device [finite state machine of

some sort since the device is capable of accessing the memory] accessing the second port of the dual port FIFO), the second node capable of [by operation of the FIFO itself] independently and asynchronously performing a memory write process, of the plurality of processes, by obtaining a first copy of a memory full indicator (C 7, L 9-17); obtaining a copy of a read index [address], the read index copy indicating a read element position in the memory and when the first copy of the memory full indicator indicates that the memory is not full (C 7, L 16-17), determining an available write count from the read index copy and a write index, the write index indicating a write element position in the memory (C 7, L 16-38; C 4, L 9-67; C 5, L 1-7); beginning at the write element position, writing an amount of data corresponding to the available write count and updating the write index to indicate a next write element position based upon the amount of data written (C 6, L 35-67; C 7, L 1-5).

Claim 13 is rejected for the same rationale applied to claim 2 above.

Claim 14 is rejected for the same rationale applied to claim 3 above.

Claim 15 is rejected for the same rationale applied to claim 4 above.

Claims 16 and 19 are rejected for the same rationale applied to claim 5 above.

Claims 17-18 are rejected for the same rationale applied to claims 6-7 above.

Regarding claims 24-25 and 28, L'Ecuyer discloses while providing independent and asynchronous performance of a memory read process of a plurality of processes, providing independent and asynchronous performance of a write process of a plurality of processes, wherein the read process comprises obtaining a first copy of a memory full indicator (Figure 3,

step 51; the system sets the full flag false, however, in doing so the system establishes that the memory is not full); obtaining a copy of a write index [address], the write index copy indicating a write element position in the memory, determining an available read count from the write index copy and a read index, the read index indicating a read element position in the memory (C 5, L 51-67; C 6, L 1-8; C 3, entire); beginning at the read element position, reading a plurality of data elements corresponding to the available read count and updating the read index to indicate a next read element position (C 5, L 9-44).

Regarding claim 26, L'Ecuyer discloses subsequent to updating the read index, when the first copy of the memory full indicator indicates that the memory is full or may be full, clearing the memory full indicator to indicate that the memory is not full (C 5, L 45-48).

Claim 27 is rejected for the same rationale applied to claim 18 above.

Regarding claims 32 and 35, L'Ecuyer discloses obtaining a second copy of the memory full indicator (C 7, L 9-12); obtaining a copy of the read index and when the second copy of the memory full indicator indicates that the memory is not full, determining an available write count from the read index copy and the write index (C 7, L 16-38; C 4, L 9-67; C 5, L 1-7); beginning at the write element position indicated by the write index, writing an amount of data corresponding to the available write count and updating the write index to indicate a next write element position based upon the amount of data written (C 6, L 35-67; C 7, L 1-5).

Regarding claims 33-34, L'Ecuyer discloses determining whether the updated write index is equal to the read index and setting the memory full indicator to indicate that the memory is full or may be full (C 7, L 9-12; the procedure disclosed here occurs prior to a new write and after a prior write and thus it is evident that the value of the write address is the updated write address).

Regarding claims 36-37, 40 and 48, L'Ecuyer discloses a memory (Figure 1); a first node (process or device coupled to one of the ports of the FIFO memory, which is a finite state machine of some sort since the device is capable of accessing the memory; L'Ecuyer discloses a dual port FIFO; C 1, L 16-18); a second node coupled to the memory (the second device [finite state machine of some sort since the device is capable of accessing the memory] accessing the second port of the dual port FIFO), the second node capable of [by operation of the FIFO itself] independently and asynchronously performing a memory read process, of the plurality of processes, by obtaining a first copy of a memory full indicator (Figure 3, step 51; the system sets the full flag false, however, in doing so the system establishes that the memory is not full); obtaining a copy of a write index [address], the write index copy indicating a write element position in the memory, determining an available read count from the write index copy and a read index, the read index indicating a read element position in the memory (C 5, L 51-67; C 6, L 1-8; C 3, entire); beginning at the read element position, reading a plurality of data elements corresponding to the available read count and updating the read index to indicate a next read element position (C 5; L 9-44).

Claim 38 is rejected for the same rationale applied to claim 26 above.

Claim 39 is rejected for the same rationale applied to claim 27 above.

Claim 44 is rejected for the same rationale applied to claim 32 above.

Claim 45 is rejected for the same rationale applied to claim 33 above.

Claim 46 is rejected for the same rationale applied to claim 34 above.

Claim 47 is rejected for the same rationale applied to claim 35 above.

Allowable Subject Matter

5. Claim 49 is allowed.

6. Claims 9-11, 20-22, 29-31, 41-43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

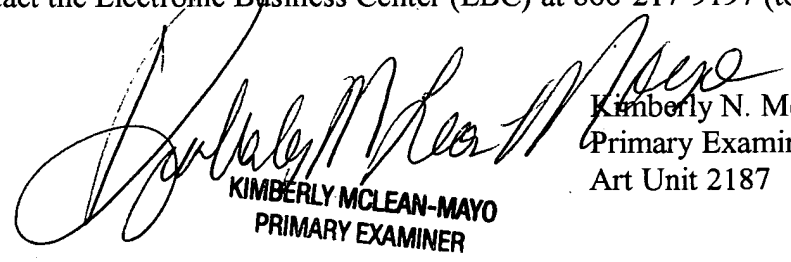
7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Secatch – PGPUB: US 2003/0131162 – predetermined read and write count FIFO system.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 571-272-4194. The examiner can normally be reached on Mon, Wed, Thurs (10-4), Tues (9:45 - 6:15).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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Primary Examiner
Art Unit 2187

KNM

March 18, 2006